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PATENT APPLICATION

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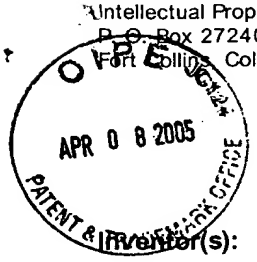


**IN THE**
**UNITED STATES PATENT AND TRADEMARK OFFICE**

**Inventor(s):** John R. McVey et al.

**Confirmation No.:** 4745

**Application No.:** 09/541771

**Examiner:** Twyler Lamb

**Filing Date:** Apr 03, 2000

**Group Art Unit:** 2622

**Title:** A Method And Device For Improving Utilization Of A Bus

**Mail Stop Appeal Brief-Patents**
**Commissioner For Patents**
**PO Box 1450**
**Alexandria, VA 22313-1450**

**TRANSMITTAL OF APPEAL BRIEF**

**Sir:**

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **Feb. 17, 2005**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

**(complete (a) or (b) as applicable)**

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

| | | |
|---|---|---|
| ( ) | one month | $120.00 |
| ( ) | two months | $450.00 |
| ( ) | three months | $1020.00 |
| ( ) | four months | $1590.00 |

( ) The extension fee has already been filled in this application.

**(X)** (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

**(X)** I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on **Apr. 8, 2005** and is addressed to the Commissioner for Patents, Alexandria, VA 22313-1450

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Respectfully submitted,

**John R. McVey et al.**

By

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Date: **Apr. 8, 2005**

Telephone No.: **360 212 8052**

Atty. Docket No.: 10991816-1



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

| | |
|---|---|
| Appellant: | John R. McVey et al. |
| Filing Date: | 04/03/2000 |
| For: | A METHOD AND DEVICE FOR IMPROVING UTILIZATION OF A BUS |
| Group Art Unit: | 2622 |
| Docket No.: | 10991816-1 |
| Application No.: | 09/541,771 |
| Examiner: | Lamb, Twyler Marie. |

**BRIEF ON APPEAL**

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

## 1. Real Party in Interest

The real party in interest is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249, Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware corporation, headquartered in Palo Alto, California. The general or managing partner of HPDC is HPQ Holdings, LLC.

## 2. Related Appeals and Interferences

There are no related appeals or interferences that will directly affect, be directly affected by, or have a bearing on the present appeal, known to Appellant or Appellant's patent representative.

**3. Status of Claims**

Claims 2-9 and 11-34 are pending in the present application. Claims 2-9, 11-12, and 22-34 stand rejected. Claims 13-15 stand as objected to as being dependent upon a rejected base claim, but the Examiner has indicated that these claims would allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claims 16-21 have been allowed by the Examiner.

**4. Status of Amendments**

Claims 1-21 were originally pending in the application. In response to a first Office Action mailed on July 7, 2003, which was non-final, the Appellant amended the abstract to overcome an Examiner's objection to a length of the abstract. Additionally, in the office action response, the Appellant traversed the Examiner's rejections of claims 1-12 and objections to claims 13-15. In a response to a second Office Action mailed on January 5, 2004, which was non-final, the Appellant traversed the Examiner's rejections of claims 1-12 and 13-15. Additionally, the Appellant amended the application to add claims 22-34. In response to a third Office Action mailed on June 15, 2004, which was a final rejection, the Appellant amended claim 2 and claim 11 and canceled claim 1 and claim 10. The Appellant filed the response to the third Office Action as a Request for Continued Examination. This is an appeal from the fourth Office Action mailed on November 4th, 2004, which was a final rejection, rejecting claims 2-9 and 11-12, and 22-34. No amendments have been filed subsequent to the final rejection mailed on November 4$^{th}$, 2004.

**5. Summary of the Claimed Subject Matter**

Claimed subject matter relates generally to methods for performing a transaction on a bus and a system including a bus management device (see for example page 1, line 29 through page 2, line 4 and page 2, lines 5-14 of the specification). Typically, memory devices do not generate outputs used for handshaking operations in sending or receiving data. (see for example page 1, lines 14-15 of the specification) In systems using these types of memory devices, the handshaking operations in data transfers involving the memory devices are performed by the memory controller (see for example page 1, lines 15-17 of the specification). Memory controllers frequently include internal

hardware, such as counters or timers, which perform a timing function to ensure that control signals, address information, or data is delivered to or taken from the appropriate bus at the correct time (see for example page 1, lines 17-20 of the specification). When different types of memory devices are used in the system, this can lead to complexity because of the different timing used by different memory devices (see for example page 1, lines 20-23 of the specification). In addition, using memory devices having different timing characteristics can result in reduced utilization of the bus (see for example page 1, lines 23-25 of the specification).

Claim 2

Claim 2 is directed to a method for performing a transaction on a bus (see for example in one embodiment, page 10, lines 27-28, of the specification referring to performing transactions such as reads and writes over processor data bus 46). The method includes receiving a signal requesting the transaction (see, for example in one embodiment, page 11, lines 25-29 of the specification and Fig. 1, referring to memory controller 12 accessing the data specifying the number of clock cycles of usage and providing this information to bus management device). The method further includes generating a first value using the signal (see, for example in one embodiment, page 11, lines 29-31and Fig. 1 of the specification referring to bus management device 11 using information received from memory controller 12 to change the value stored in the storage device to reflect the scheduling of this transaction over memory data bus 50). The method also includes storing the first value in a storage device, with the first value including a plurality of bits and with those of the plurality of bits in a first state corresponding to clock cycles during which the usage of the bus occurs for the transaction (see, for example in one embodiment, page 11, lines 29-31 and page 12, lines 4-7 and Fig. 1 of the specification referring to bus management device 11 changing the value stored in the storage device and referring to changing the value in the storage device so that a number of bits of the value equal to the number of clock cycles during which valid data is present on memory data bus 50 will be set to an asserted state).

Claim 4

Claim 4 is indirectly dependent upon claim 2 and recites that receiving the signal includes receiving a second value indicating a number of the clock cycles during which the usage of the bus occurs for the transaction (see, for example in one embodiment, Fig. 1 and page 11, lines 25-29 of the specification referring to memory controller 12 accessing the data specifying the number of clock cycles of usage of memory data bus 50 and providing this information to bus management device 11). Claim 4 also recites that generating the first value includes generating the plurality of bits using the second value (see, for example in one embodiment, page 12, lines 4-7 and Fig. 1 of the specification referring to the value in the storage device changing so that a number of bits of the value equal to the number of clock cycles during which valid data is present on memory data bus 50 will be set to an asserted state).

Claim 5

Claim 5 is dependent upon claim 4 and recites changing the first value in the storage device after storing the value and after the occurrence of at least one of the clock cycles by shifting ones of the plurality of bits between the storage elements (see, for example in one embodiment, Fig. 2, Fig. 3F and page 19, lines 22-23 of the specification referring to the passage of each cycle of the clock and the shifting of bits in register 138 being shifted to the right).

Claim 7

Claim 7 is dependent upon claim 6 and recites that those of the plurality of bits in a second state indicate the clock cycles during which the bus exists in an idle condition (see, for example in one embodiment, Fig. 2 and page 16, lines 29-30 of the specification referring to a value "0" indicating that data bus 110 is not in use during the corresponding clock cycle). Claim 7 also recites that generating the first value includes generating the plurality of bits in the second state so that the bus exists in the idle condition for at least one of the clock cycles between the usage of the bus for the transaction and the usage of the bus for a previous transaction (see, for example in one embodiment, Fig. 2 and page 17, lines 27-29 of the specification referring to the location

of the bits set to a logic 1 in register 138 will be one clock cycle after the end of the usage of data 110 for the previous transaction.)

Claim 11

Claim 11 is directed to a system including a bus (see, for example in one embodiment, Fig. 2 and page 15, line 30 of the specification referring to data bus 110). Claim 11 recites a processor configured to receive first data from the bus (see, for example in one embodiment, Fig. 2 and page 16, lines 16-17 of the specification referring to accessing of DRAM 118, SRAM 122, and ROM 126 by processor 104). Claim 11 also recites a first memory device configured to send the first data to the bus (see, for example in one embodiment, Fig. 2 and page 16, lines 16-17 of the specification). Claim 11 further recites a memory controller coupled to the processor and the memory device and configured to control transfer of the first data over the bus (see, for example in one embodiment, Fig. 2 and page 16, lines 19-21 of the specification referring to memory controller 102 managing data transfers). Additionally, claim 11 recites a bus management device arranged to receive a first value from the memory controller indicating a number of clock cycles with the first data on the bus (see, for example in one embodiment, Fig. 2 and page 17, lines 21-23 of the specification referring to the information including the number of clock cycles for which valid data will be present on data bus 110 during the transaction). Claim 11 also recites that the bus management device includes a storage device to store a second value including a first plurality of bits, with positions within the second value of those of the first plurality of bits in a first state corresponding to clock cycles during which the first data exists on the bus (see, for example in one embodiment, Fig. 2 and page 17, lines 25-27 of the specification referring to bus management device 137 setting a number of bits in register 138 to a logic 1 equal to the number of clock cycles that data bus 110 will be used in the transaction).

Claim 12

Claim 12 is dependent upon claim 11 and recites those of the first plurality of bits in a second state indicate the clock cycles during which the bus exists in an idle

condition (see, for example in one embodiment, Fig. 2 and page 16, lines 29-30 of the specification referring to a value of "0" indicating that data bus 110 is not in use during the corresponding clock cycle). Claim 12 further recites that the bus management device includes a configuration to detect a change in one of the positions within the second value from the first state to the second state and to signal the memory controller to begin a first access to the first memory device a first time period before the clock cycles corresponding to those of the first plurality of bits in the first state begin (see, for example in one embodiment, Fig. 2 and page 18, lines 4-10 of the specification referring to bus management device 137 checking a bit position in register 138 to determine when the 0 corresponding to the clock cycle between usage time periods of data bus 110 on successive transactions is shifted into this position and bus management device 137 signaling memory controller 102 that the control phase of the corresponding transaction should begin).

Claim 22

Claim 22 is directed to a method and recites scheduling a first transaction including usage of a bus by setting a first plurality of bits to a level (see, for example in one embodiment, Fig. 2 and page 17, lines 24-27 of the specification referring to bus management device 137 setting a number of bits in register 138 to a logic 1 equal to the number of clock cycles that data bus 110 will be used in the transaction). Claim 22 also recites each of the first plurality of bits set to the level indicating the usage of the bus during a corresponding one of a first plurality clock cycles to occur (see, for example, in one embodiment, Fig. 2 and page 16, lines 28 through page 17 line 1 of the specification referring to a value of "1" in a bit position indicates that data bus 110 has valid data during the corresponding clock cycle, a value of "0" indicates that data bus 110 is not in use during the corresponding clock cycle, and referring to each bit of the register 138 represents activity on the data bus 110 in a single clock cycle). Claim 22 further recites scheduling a second transaction including usage of the bus by setting a second plurality of bits to the level (see, for example in one embodiment, Fig. 2 and page 17, lines 24-27 of the specification referring to bus management device 137 setting a number of bits in register 138 to a logic 1 equal to the number of clock cycles

that data bus 110 will be used in the transaction). Claim 22 also recites each of the second plurality of bits set to the level indicating the usage of the bus during a corresponding one of a second plurality of clock cycles (see, for example, in one embodiment, Fig. 2 and page 16, lines 28 through page 17 line 1 of the specification referring to a value of "1" in a bit position indicates that data bus 110 has valid data during the corresponding clock cycle, a value of "0" indicates that data bus 110 is not in use during the corresponding clock cycle, and referring to each bit of the register 138 represents activity on the data bus 110 in a single clock cycle). Claim 22 further indicates the second plurality of clock cycles occurs after the first plurality of clock cycles (see, for example in one embodiment, Fig. 2, Fig. 3A, and page 18, lines 17-31 of the specification referring to a value in a register 138 for a transaction in which data bus 110 is to be used for 4 clock cycles and referring to after the transaction corresponding to the 4 lowest order bits shown in Figure 3A is completed, there is one clock cycle of delay before beginning a read access of one word using data bus 110 for one clock cycle).

Claim 27

Claim 27 is indirectly dependent upon claim 22. Claim 27 recites a first lowest order bit of the first plurality of bits corresponds to a beginning of a first transaction on the bus (see, for example in one embodiment, Fig. 2, Fig. 3A, and page 18, lines 25-26 of the specification referring to the lowest order bit of register 138 corresponding to the first clock cycle of the access). Claim 27 also recites a second lowest order bit of the second plurality of bits corresponds to a beginning of a second transaction on the bus (see, for example in one embodiment, Fig. 2, Fig. 3A, and page 18, lines 29-30 of the specification referring to beginning a read access of one word, indicated by bit 5 of register 138 set to a logic 1).

Claim 28

Claim 28 is dependent upon claim 22. Claim 28 recites a first number of the first plurality of bits corresponds to a first length of time of the usage of the bus for a first transaction in terms of clock cycles in the first plurality of clock cycles (see, for example

in one embodiment, Fig. 2, Fig. 3A, and page 18, lines 16-19 of the specification referring to the value in register 138 for a transaction in which data bus 110 is to be used for 4 clock cycles as indicated by bits 0-3 of register 138 set to a logic 1). Claim 28 also recites a second number of the second plurality of bits corresponds to a second length of time of the usage of the bus for a second transaction in terms of clock cycles in the second plurality of clock cycles (see, for example in one embodiment, Fig. 2, Fig. 3A, and page 18, lines 29-31 of the specification referring to beginning a read access of one word (indicated by bit 5 of register 138 set to a logic 1) using data bus 110 for one clock cycle).

Claim 32

Claim 32 is an independent claim directed to an apparatus. The "means for" element of claim 32 is intended to invoke interpretation according to 35 U.S.C. section 112, sixth paragraph. Claim 32 recites a means for determining a value including a plurality of bits with those of the plurality of bits at a first level indicating usage of a bus during a first set of corresponding clock cycles and with those of the plurality of bits at a second level indicating no usage of the bus during a second set of corresponding clock cycles (see, for example in one embodiment Fig. 4, Fig. 5A-5G disclosing the hardware description language code that defines the logic to implement Fig. 4, Fig. 3E, Fig. 3F showing a representation of successive values stored in register 138 corresponding to cycles of the clock shown in Fig. 3E, and page 23 line 10 through page 26 line 24 of the specification referring to in particular, among other things, a transaction so that Busy0 400 would receive 2 successive groups of 8 bits each set to a logic 1 (page 24, lines 12-13) and referring to each of the storage elements includes a reset input used to initialize the value in the register to 0 (page 25, lines 6-7). Claim 32 also recites a storage device to store the plurality of bits (see, for example in one embodiment Fig. 4 and page 24, lines 29-31 referring to block 408 representing the 15 storage elements and referring to flip flop 410 as representative of the storage elements).

Claim 34

Claim 34 is dependent upon claim 32. The "means for" element of claim 32 is intended to invoke interpretation according to 35 U.S.C. section 112, sixth paragraph. Claim 34 recites that the means for determining a value includes a configuration to change the plurality of bits in the storage device according to occurrence of ones of the first set of corresponding clock cycles and ones of the second set of corresponding cycles (see, for example in one embodiment Fig. 4 and page 25, lines 8-21 of the specification referring to a shift right by one bit being executed by the storage elements in the register for a clock cycle).

## 6. Grounds of Rejection to be Reviewed on Appeal

The issues on appeal are whether the Examiner erred in rejecting Claims 2-6, and 11 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,032,214 (issued to Farmwald et al.) and whether the Examiner erred in rejecting Claims 7-9, 12 and 22-34 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,032,214 (Farmwald et al.) in view of U.S. Patent No. 5,581,782 (issued to Sarangdhar et al.).

## 7. Argument

### I. Legal Standards

### A. Standards Under 35 U.S.C. § 102(b).

Claims 2-6, and 11 have been rejected under 35 U.S.C. § 102(b), which states:

> A person shall be entitled to a patent unless—
>
> the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States

Under Section 102, a claim is anticipated, i.e., rendered not novel, when a prior art reference discloses every limitation of the claim. In re Schreiber, 128 F.3rd 1473, 1477 (Fed. Cir. 1997). Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so." In re Mills, 916 F.2d 680, 682 (Fed. Cir. 1990). "Rejections under 35 U.S.C. § 102(a) are proper only when the claimed subject matter is identically disclosed or described in the prior art." In re Arkley, Eardley, and Long, 172 U.S.P.Q. 524, 526 (CCPA 1972).

Claim terms will be given their ordinary and accustomed meaning, unless there is "an express intent to impart a novel meaning to [the] claim [term]" by the patentee. York Prods., Inc. v. Cent. Tractor Farm & Family Ctr., 99 F.3d 1568, 1572 (Fed. Cir. 1996); Sage Prods. v. Devon Indus., Inc., 126 F.3d 1420, 1423 (Fed. Cir. 1997). The ordinary and accustomed meaning of a claim term is determined by reference to dictionaries, encyclopedias, and treatises available at the time of the patent. See Texas Digital Systems, Inc., 308 F.3d at 1203. Such references are always available for claim construction purposes and are neither extrinsic nor intrinsic evidence. See Texas Digital Systems, Inc. v. Telegenix, Inc., 308 F.3d 1193, 1202-03 (Fed. Cir. 2002).

In order to impart a specific meaning to a claim term, i.e., for the inventor to be her own lexicographer, such lexicography must appear "with reasonable clarity, deliberateness, and precision." In re Paulsen, 30 F.3d 1475, 1480 (Fed. Cir. 1994). However, intrinsic evidence may be consulted to determine the definite meaning of a claim term that is unclear. CCS Fitness, Inc. v. Brunswick Corp., 288 F.3d 1359, 1367 (Fed. Cir. 2002). A claim term may be redefined without any express statement of redefinition in the specification. Bell Atl. Network Servs., Inc. v. Covad Communications Group, Inc., 262 F.3d 1258, 1268 (Fed. Cir. 2001). "[A] claim term will not carry its ordinary meaning if the intrinsic evidence shows that the patentee distinguished that term from prior art on the basis of a particular embodiment" or "described a particular embodiment as important to the invention."

**B. Standards Under 35 U.S.C. § 103(a).**

Claims 7-9, 12, and 22-34 have been rejected under 35 U.S.C. § 103(a), which states:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The legal standards under 35 U.S.C. § 103(a) are well-settled. Obviousness under 35 U.S.C. § 103(a) involves four factual inquires: 1) the scope and content of the prior art; 2) the differences between the claims and the prior art; 3) the level of ordinary skill in the pertinent art; and 4) secondary considerations, if any, of nonobviousness. See Graham v. John Deere Co., 383 U.S. 1, 148 U.S.P.Q. 459 (1966).

In proceedings before the Patent and Trademark Office, the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. In re Piasecki, 745 F.2d 1468, 1471-72, 223 U.S.P.Q. 785, 787-88 (Fed. Cir. 1984). "'[The Examiner] can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references.'" In re Fritch, 972 F.2d 1260, 1265, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992).Under 35 U.S.C. § 103, the test for obviousness is whether the claimed invention as a whole, in light of all the teaching of the references in their entireties, would have been obvious to one of ordinary skill in the art at the time the invention was made. 35 U.S.C. § 103; *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1549, 220 U.S.P.Q. 193, 199 (Fed. Cir. 1983).

The Manual of Patent Examining Procedure states the following with respect to the elements of an obviousness rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves

or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). ***MPEP § 706.02(j)*** (emphasis added).

As noted by the Federal Circuit, the "factual inquiry whether to combine references must be thorough and searching." McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 60 U.S.P.Q. 2d 1001 (Fed. Cir. 2001). Further, it "must be based on objective evidence of record." In re Lee, 277 F.3d 1338, 61 U.S.P.Q. 2d 1430 (Fed. Cir. 2002). The teaching or suggestion to make the claimed combination must be found in the prior art, and not in the applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q. 2d 1438 (Fed. Cir. 1991). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 U.S.P.Q. .2d 1430 (Fed. Cir. 1990). "It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to '[use] that which the inventor taught against its teacher.'" Lee (citing W.L. Gore v. Garlock, Inc., 721 F.2d 1540, 1553, 220 U.S.P.Q. 303, 312-13 (Fed. Cir. 1983)). Teaching away from the claimed invention is a strong indication of non-obviousness and an improper combination of references. U.S. v. Adams, 383 U.S. 39 (1966).

**II. The Examiner's Rejection of Claims 2-6, and 11 Under 35 U.S.C. § 102(b) as Being Anticipated by U.S. Patent No. 6,032,214 (Farmwald et al.) Should be Reversed Because the Sections of Farmwald et al Relied Upon by the Examiner Do Not Teach at Least One Limitation of Each of these Claims.**

The claimed invention is not anticipated under § 102 unless each and every element of the claimed invention is found in the prior art. (Hydratech, Inc. v.

Monochronal Antibodies, Inc., Fed. Cir. 1986). Accordingly, the rejection of these claims under 35 U.S.C. § 102(b) is improper and should be reversed.

**A. Claims 2 and 3 Are Patentable Over Farmwald et al Because the Sections of Farmwald et al Relied Upon by the Examiner Do Not Disclose storing a first value in a storage device, with the first value including a plurality of bits and with those of the plurality of bits in a first state corresponding to clock cycles during which the usage of the bus occurs for the transaction.**

In the fourth Office Action mailed on November 4th, 2004, which was a final rejection, the Examiner seems to assert that the limitations of claim 2 recited in the paragraph heading above read upon column 9, lines 21-36 and column 12, line 56 through column 13, line 3 of Farmwald et al. (on page 2, item 2 of the fourth office action). Additionally, at pages 6-7, item 8 of the fourth Office Action, the Examiner seems to assert that at least some of the limitations recited in the paragraph heading above read upon column 6 line 52 through column 7 line 5 of Farmwald et al.

Farmwald et al at column 9, lines 21-36 discloses, among other things, a "request packet 22" containing "6 bytes of data—4.5 address bytes and 1.5 control bytes" and discloses that "[s]etting 23 AddrValid=1 in an otherwise unused cycle indicates the start of an request packet (control information)". And, Farmwald et al at column 12, line 56 through column 13, line 3 discloses, among other things, " [a] simple method is for each master to maintain a bus-busy data structure, for example by maintaining two pointers, one to indicate the earliest point in the future when the bus will be busy and the other to indicate the earliest point in the future when the bus will be free, that is, the end of the latest pending data block transfer. Using this information, each master can determine whether and when there is enough time to send a request packet (as described above under Protocol) before the bus becomes busy with another data block transfer and whether the corresponding data block transfer will interfere with pending bus transactions. Thus each master must read every request packet and update its bus-busy data structure to maintain information about when the bus is and will be free."

Farmwald et al at column 6 line 52 through column 7 line 5 discloses, among other things, initiating "a bus transaction by sending a request packet (a sequence of bytes comprising address and control information) to one or more slave devices on the bus." It additionally discloses that an "address can consist of 16 to 40 or more bits", "each slave on the bus must decode the request packet to see if that slave needs to respond to the packet", and "after a specified access time the slave(s) respond by returning one or more bytes (8 bits) of data or by storing information made available from the bus." Furthermore, this section of Farmwald et al discloses that "a request packet and the corresponding bus access are separated by a selected number of bus cycles, allowing the bus to be used in the intervening bus cycles by the same or other masters for additional requests or brief bus accesses."

At page 2, item 2 of the fourth Office Action, the Examiner seems to be asserting that the "first value" recited in claim 2 reads upon disclosure of Farmwald et al in column 9, lines 21-36. More specifically, the Examiner seems to be asserting that the first value reads upon the "request packet 22". But, there is no teaching or suggestion in this section of Farmwald et al that the 6 bytes contained in "request packet 22" include a "plurality of bits and with those of those of the plurality of bits in a first state corresponding to clock cycles during which the usage of the bus occurs for the transaction". Rather, column 6 line 52 through column 7 line 5 of Farmwald et al seems to indicate that the request packet is decoded by each slave on the bus to see if that slave needs to respond to the packet. The slave that the packet is directed to must then begin any internal processes needed to carry out the requested bus transaction at the requested time. Nowhere in these sections of Farmwald et al is there a teaching or suggestion that those of a plurality of bits of the request packet 22 in a first state correspond to clock cycles during which usage of the bus occurs.

Additionally, with respect to column 12 line 56 through column 13 line 3 of Farmwald et al, there is no teaching in this section of Farmwald et al that the "two pointers" "indicate the earliest point in the future when the bus will be busy" and "the earliest point in the future when the bus will be free" by using a "bus-busy data structure" including a plurality of bits and with those of the plurality of bits in a first state

corresponding to clock cycles during which the usage of the bus occurs for the transaction. Rather, this section of Farmwald et al suggests, in generalized, relatively non-specific terms, that each master could keep track of when a bus is and will be busy. Therefore, the rejection of claim 2 under 35 U.S.C. § 102(b) based upon Farmwald et al is improper and should be reversed for at least this reason. Claim 3 is dependent upon claim 2 and the rejection of claim 3 under 35 U.S.C. § 102(b) based upon Farmwald et al is improper and should be reversed for at least the same reason as discussed for claim 2.

**B. Claim 4 is Patentable Over Farmwald et al Because the Sections of Farmwald et al Relied Upon by the Examiner Do Not Disclose positions within the first value of those of the plurality of bits in the first state indicating the clock cycles during which the usage of the bus occurs for the transaction.**

In the fourth Office Action mailed on November 4th, 2004, which was a final rejection, at page 3, item 2, the Examiner seems to assert that limitations of claim 4 recited in the paragraph heading above read upon column 12 lines 56 through column 13 line 3 of Farmwald et al.

Farmwald et al at column 12 line 56 through column 13 line 3 discloses, among, other things, "a simple method is for each master to maintain a bus-busy data structure, for example by maintaining two pointers, one to indicate the earliest point in the future when the bus will be busy and the other to indicate the earliest point in the future when the bus will be free, that is, the end of the latest pending data block transfer" and "each bus master must read every request packet and update its bus-busy data structure to maintain information about when the bus is and will be free."

There is no teaching in this section of Farmwald et al that the "two pointers" "indicate the earliest point in the future when the bus will be busy" and "the earliest point in the future when the bus will be free" by using those positions of bits within the "bus-busy data structure" in a first state to indicate the clock cycles during which the usage of the bus occurs for the transaction. Rather, this section of Farmwald et al suggests, in generalized, relatively non-specific terms, that each master could keep track of when a

bus is and will be busy. Therefore, the rejection of claim 4 under 35 U.S.C. § 102(b) based upon Farmwald et al is improper and should be reversed for at least this reason.

**C. Claims 5 and 6 Are Patentable Over Farmwald et al Because the Sections of Farmwald et al Relied Upon by the Examiner Do Not Disclose changing the first value in the storage device after storing the first value and after an occurrence of at least one of the clock cycles by shifting ones of the plurality of bits between the storage elements.**

In the fourth Office Action mailed on November 4th, 2004, which was a final rejection, at page 3, item 2, the Examiner seems to assert that limitations of claim 5 read upon column 15, lines 6-23 of Farmwald et al.

Farmwald et al at column 15 lines 6-23 discloses, among, other things "a four-stage reset shift register", "a first reset signal . . . causes the device to hard reset, for example by clearing all internal registers and resetting all state machines", and " a second reset signal . . . causes that device to latch the contents of the external bus into the internal device ID register."

There is no disclosure in this section of Farmwald et al that the "four stage reset shift register" changes the "ResetIn" value after an occurrence of at least one of the clock cycles by shifting ones of the plurality of bits that may be included in the "ResetIn" value between storage elements in the "four stage reset shift register". Additionally, there is no disclosure in this section of Farmwald et al that the "ResetIn" value includes a plurality of bits and with those of the plurality of bits in a first state corresponding to clock cycles during which the usage of the bus occurs. Furthermore, as indicated previously with respect to the Appellants arguments against the rejection of claim 2, the Examiner seems to be asserting that "the first value" reads upon the "request packet 22". It appears from this section of Farmwald et al that the value latched into the "a four-stage reset shift register" is related to device ID information, not "request packet 22". Therefore, the rejection of claim 5 under 35 U.S.C. § 102(b) based upon Farmwald et al is improper and should be reversed for at least this reason. Claim 6 is dependent upon claim 5 and the rejection of claim 6 under 35 U.S.C. § 102(b) based upon

Farmwald et al is improper and should be reversed for at least the same reason as discussed for claim 5.

**D. Claim 11 Is Patentable Over Farmwald et al Because the Sections of Farmwald et al Relied Upon by the Examiner Do Not Disclose a bus management device including a storage device to store a second value including a first plurality of bits, with positions within the second value of those of the first plurality of bits in a first state corresponding to clock cycles during which the first data exists on the bus.**

In the fourth Office Action mailed on November 4th, 2004, which was a final rejection, the Examiner seems to assert that the limitations of claim 11 recited in the paragraph heading above read upon column 9, lines 21-36 and column 12, line 56 through column 13, line 3 of Farmwald et al. (on page 2, item 2 of the fourth office action). Additionally, at pages 6-7, item 8 of the fourth Office Action, the Examiner seems to assert that at least some of the limitations recited in the paragraph heading above read upon column 6 line 52 through column 7 line 5 of Farmwald et al.

Farmwald et al at column 9, lines 21-36 discloses, among other things, a "request packet 22" containing "6 bytes of data—4.5 address bytes and 1.5 control bytes" and discloses that "[s]etting 23 AddrValid=1 in an otherwise unused cycle indicates the start of an request packet (control information)". And, Farmwald et al at column 12, line 56 through column 13, line 3 discloses, among other things, " [a] simple method is for each master to maintain a bus-busy data structure, for example by maintaining two pointers, one to indicate the earliest point in the future when the bus will be busy and the other to indicate the earliest point in the future when the bus will be free, that is, the end of the latest pending data block transfer. Using this information, each master can determine whether and when there is enough time to send a request packet (as described above under Protocol) before the bus becomes busy with another data block transfer and whether the corresponding data block transfer will interfere with pending bus transactions. Thus each master must read every request packet and

update its bus-busy data structure to maintain information about when the bus is and will be free."

Farmwald et al at column 6 line 52 through column 7 line 5 discloses, among other things, initiating "a bus transaction by sending a request packet (a sequence of bytes comprising address and control information) to one or more slave devices on the bus." It additionally discloses that an "address can consist of 16 to 40 or more bits", "each slave on the bus must decode the request packet to see if that slave needs to respond to the packet", and "after a specified access time the slave(s) respond by returning one or more bytes (8 bits) of data or by storing information made available from the bus." Furthermore, this section of Farmwald et al discloses that "a request packet and the corresponding bus access are separated by a selected number of bus cycles, allowing the bus to be used in the intervening bus cycles by the same or other masters for additional requests or brief bus accesses."

At page 2, item 2 of the fourth Office Action, the Examiner, by analogy, seems to be suggesting that the "second value" recited in claim 11 reads upon disclosure of Farmwald et al in column 9, lines 21-36. More specifically, the Examiner seems to be asserting that the second value reads upon the "request packet 22". But, there is no teaching or suggestion in this section of Farmwald et al that the 6 bytes contained in "request packet 22" include a "second value including a first plurality of bits, with positions within the second value of those of the first plurality of bits in a first state corresponding to clock cycles during which the first data exists on the bus". Rather, column 6 line 52 through column 7 line 15 of Farmwald et al seems to indicate that the request packet is decoded by each slave on the bus to see if that slave needs to respond to the packet. The slave that the packet is directed to must then begin any internal processes needed to carry out the requested bus transaction at the requested time. Nowhere in these sections of Farmwald et al is there a teaching or suggestion of positions within the request packet 22 of those of the first plurality of bits in a first state corresponding to clock cycles during which the first data exists on the bus. Additionally, with respect to column 12 line 56 through column 13 line 3 of Farmwald et al, there is no teaching in this section of Farmwald et al that the "two pointers" "indicate the earliest

point in the future when the bus will be busy" and "the earliest point in the future when the bus will be free" by using the "bus-busy data structure" including a first plurality of bits, with positions within the "bus-busy data structure" of those of the first plurality of bits in a first state corresponding to clock cycles during which the first data exists on the bus. Rather, this section of Farmwald et al suggests, in generalized, relatively non-specific terms, that each master could keep track of when a bus is and will be busy. Therefore, the rejection of claim 11 under 35 U.S.C. § 102(b) based upon Farmwald et al is improper and should be reversed for at least this reason.

**III. The Examiner's Rejection of Claims 7-9, 12, and 22-34 Under 35 U.S.C § 103(a) As Being Unpatentable Over U.S. Patent No. 6,032,214 (Farmwald et al.) in view of U.S. Patent No. 5,581,782 (Sarangdhar et al) Should be Reversed Because the Claimed Invention Would Not be Obvious Over Farmwald et al. in View of and Sarangdhar et al.**

The claimed invention is not obvious under 35 U.S.C. § 103 unless the prior art reference or references teaches or suggests all of the claim limitations. In re Royka, 490 Fed. 2d 981 (CCPA 1974). Accordingly, the rejection of these claims under 35 U.S.C. § 103(a) is improper and should be reversed because there prior art references cited in the Examiner's rejections of claims 7-9, 12, and 22-34 do not teach all the limitations of these claims.

**A. Claims 7-9 are Patentable Over Farmwald et al. in View of Sarangdhar et al Because Neither Farmwald et al or Sarangdhar et al Disclose that those of the plurality of bits in a second state indicate the clock cycles during which the bus exists in an idle condition and that generating the first value includes generating the plurality of bits in the second state so that the bus exists in the idle condition for at least one of the clock cycles between the usage of the bus for the transaction and the usage of the bus for a previous transaction.**

In the fourth Office Action mailed on November 4th, 2004, which was a final rejection, the Examiner seems to assert, on page 4, item 4, that the limitations of claim 7 read upon column 2, line 63 through column 3, line 17 of Sarangdhar et al.

Sarangdhar et al at column 2, line 63 through column 3, line 17 discloses, among other things "[a]nother element that may be included is an ownership state indicator that indicates the ownership state of the system bus", "[i]f the ownership state is a first state the symmetric arbitrator of each processor selects the bus owner at least one clock cycle earlier than if the ownership state is a second state", and "[t]he first and second states can be idle and busy states, respectively." The cited section of Sarangdhar et al seems to relate to arbitrating for selection of a bus owner. If the "ownership state indicator" referenced in this section of Sarangdhar et al is in a "first state", the "bus owner" is selected at least one clock cycle earlier than if the ownership state is a second state. The Appellants assert that the reference to the "first state" as "idle" and the "second state" as "busy" relates to column 9, lines 19-22 of Sarangdhar et al which discloses "a symmetric ownership state bit that describes whether the bus ownership is being retained by the current symmetric owner ("busy" state) or is in a state where no symmetric agent currently owns the bus ("idle" state)."

The Examiner seems to be asserting that the "plurality of bits in a second state indicate the clock cycles during which the bus exists in an idle condition" recited in claim 7 read upon "ownership state indicator". But, the "ownership state indicator" is directed to which "symmetric owner" has "bus ownership" (see column 9, lines 19-22 of Sarangdhar et al). The "ownership state indicator" does not indicate the clock cycles during which the bus exists in an idle condition as recited in claim 7.

The Examiner also seems to be asserting that the limitations of claim 7 reciting "generating the plurality of bits in the second state so that the bus exists in the idle condition for at least one of the clock cycles between the usage of the bus for the transaction and the usage of the bus for a previous transaction" reads upon column 3, lines 13-17 of Sarangdhar et al which discloses "[i]f the ownership state is a first state the symmetric arbitrator of each processor selects the bus owner at least one clock cycle earlier than if the ownership state is a second state", and "[t]he first and second states can be idle and busy states, respectively." However, this section of Sarangdhar et al is referring to the "symmetric arbitrator of each processor" selecting "the bus owner at least one clock cycle earlier" depending upon whether the ownership state is a first state or a second state. So, this section of Sarangdhar et al is disclosing when bus

ownership occurs for the symmetric arbitrator. This section of Sarangdhar et al is not disclosing that by setting the "ownership state indicator" the bus exists in an idle condition for at least one of the clock cycles between a transaction and a previous transaction.

Nowhere in column 2, line 63 through column 3, line 17 of Sarangdhar et al is it disclosed that a plurality of bits in a second state indicate the clock cycles during which the bus exists in an idle condition and that generating the first value includes generating the plurality of bits in the second state so that the bus exists in the idle condition for at least one of the clock cycles between the usage of the bus for the transaction and the usage of the bus for a previous transaction. Therefore, the rejection of claim 7 under 35 U.S.C. § 103(a) is improper and should be reversed because the prior art references cited in the Examiner's rejection of claim 7 do not teach all the limitations of this claim. Claims 8-9 are dependent upon claim 7 and the rejections of claims 8-9 under 35 U.S.C. § 103(a) based upon Farmwald et al in view of Sarangdhar et al is improper and should be reversed for at least the same reason as discussed for claim 7.

**B. Claim 12 is Patentable Over Farmwald et al. in View of Sarangdhar et al Because Neither Farmwald et al or Sarangdhar et al Disclose that those of the first plurality of bits in a second state indicate the clock cycles during which the bus exists in an idle condition and that the bus management device includes a configuration to detect a change in one of the positions within the second value from the first state to the second state and to signal the memory controller to begin a first access to the first memory device a first time period before the clock cycles corresponding to those of the first plurality of bits in the first state begin.**

In the fourth Office Action mailed on November 4th, 2004, which was a final rejection, the Examiner seems to assert that the limitations of claim 12 read upon column 2, line 63 through column 3, line 17 of Sarangdhar et al. Sarangdhar et al at column 2, line 63 through column 3, line 17 discloses, among other things, "[a]nother element that may be included is an ownership state indicator that indicates the ownership state of the system bus", "[i]f the ownership state is a first state the symmetric arbitrator of each processor selects the bus owner at least one clock cycle

earlier than if the ownership state is a second state", and "[t]he first and second states can be idle and busy states, respectively." The cited section of Sarangdhar et al seems to relate to arbitrating for selection of a bus owner. If the "ownership state indicator" referenced in this section of Sarangdhar et al is in a "first state", the "bus owner" is selected at least one clock cycle earlier than if the ownership state is a second state. The Appellants assert that the reference to the "first state" as "idle" and the "second state" as "busy" relates to column 9, lines 19-22 of Sarangdhar et al which discloses "a symmetric ownership state bit that describes whether the bus ownership is being retained by the current symmetric owner ("busy" state) or is in a state where no symmetric agent currently owns the bus ("idle" state)."

The Examiner seems to be asserting that the "first plurality of bits in a second state indicate the clock cycles during which the bus exists in an idle condition" recited in claim 12 read upon "ownership state indicator". But, the "ownership state indicator" is directed to which "symmetric owner" has "bus ownership" (see column 9, lines 19-22 of Sarangdhar et al). The "ownership state indicator" does not indicate the clock cycles during which the bus exists in an idle condition as recited in claim 12.

The Appellants are not clear on what the Examiner is asserting that the limitations of claim 12 reciting "the bus management device includes a configuration to detect a change in one of the positions within the second value from the first state to the second state and to signal the memory controller to begin a first access to the first memory device a first time period before the clock cycles corresponding to those of the first plurality of bits in the first state begin" reads upon in the sections of Sarangdhar et al cited by the Examiner in page 4, item 4 of the fourth Office Action mailed on November 4th, 2004. Perhaps, as seemed to be for claim 7, the Examiner is referring to column 3, lines 13-17 of Sarangdhar et al which discloses "[i]f the ownership state is a first state the symmetric arbitrator of each processor selects the bus owner at least one clock cycle earlier than if the ownership state is a second state", and "[t]he first and second states can be idle and busy states, respectively." If this is the case, the Examiner may be asserting that "the second value" recited in claim 12 reads upon the "ownership state indicator". However, this section of Sarangdhar et al is referring to the "symmetric arbitrator of each processor" selecting "the bus owner at least one clock

cycle earlier" depending upon whether the ownership state is a first state or a second state. So, this section of Sarangdhar et al is disclosing when bus ownership occurs for the symmetric arbitrator. This section of Sarangdhar et al is not disclosing that by detecting a change in one of the positions within the "ownership state indicator" a memory controller is signaled to begin an access to a memory device as indicated in claim 12. This section of Sarangdhar et al is also not disclosing that the "ownership state indicator" is used to time access to the memory so that it begins a time period before the clock cycles corresponding to those of the first plurality of bits in the first state begin as indicated in claim 12.

Nowhere in column 2, line 63 through column 3, line 17 of Sarangdhar et al is it disclosed that a bus management device includes a configuration to detect a change in one of the positions within the second value from the first state to the second state and to signal the memory controller to begin a first access to the first memory device a first time period before the clock cycles corresponding to those of the first plurality of bits in the first state begin. Therefore, the rejection of claim 12 under 35 U.S.C. § 103(a) is improper and should be reversed because the prior art references cited in the Examiner's rejection of claim 12 do not teach all the limitations of this claim.

**C. Claim 22-26 are Patentable Over Farmwald et al. in View of Sarangdhar et al Because Neither Farmwald et al or Sarangdhar et al Disclose scheduling a first transaction including usage of a bus by setting a first plurality of bits to a level, with each of the first plurality of bits set to the level indicating the usage of the bus during a corresponding one of a first plurality clock cycles to occur and scheduling a second transaction including usage of the bus by setting a second plurality of bits to the level, with each of the second plurality of bits set to the level indicating the usage of the bus during a corresponding one of a second plurality of clock cycles to occur after the first plurality of clock cycles.**

On page 5, item 4, of the fourth Office Action mailed on November 4th, 2004, the Examiner stated that "[t]he limitations of claims 22-34 are met by the rejections above." Although, the Examiner does not specifically indicate the sections of Farmwald et al and

Sarangdhar et al upon which the limitations of claim 22 are asserted to read, the Appellants conclude that the sections of Farmwald et al and Sarangdhar et al cited in making the rejections of claims 7-9 and 12 are the basis of the Examiner's rejections of claims 22-34 under 35 U.S.C. § 103(a).

Farmwald et al at column 9, lines 21-36 discloses, among other things, a "request packet 22" containing "6 bytes of data—4.5 address bytes and 1.5 control bytes" and discloses that "[s]etting 23 AddrValid=1 in an otherwise unused cycle indicates the start of an request packet (control information)". And, Farmwald et al at column 12, line 56 through column 13, line 3 discloses, among other things, " [a] simple method is for each master to maintain a bus-busy data structure, for example by maintaining two pointers, one to indicate the earliest point in the future when the bus will be busy and the other to indicate the earliest point in the future when the bus will be free, that is, the end of the latest pending data block transfer. Using this information, each master can determine whether and when there is enough time to send a request packet (as described above under Protocol) before the bus becomes busy with another data block transfer and whether the corresponding data block transfer will interfere with pending bus transactions. Thus each master must read every request packet and update its bus-busy data structure to maintain information about when the bus is and will be free."

Farmwald et al at column 6 line 52 through column 7 line 5 discloses, among other things, initiating "a bus transaction by sending a request packet (a sequence of bytes comprising address and control information) to one or more slave devices on the bus." It additionally discloses that an "address can consist of 16 to 40 or more bits", "each slave on the bus must decode the request packet to see if that slave needs to respond to the packet", and "after a specified access time the slave(s) respond by returning one or more bytes (8 bits) of data or by storing information made available from the bus." Furthermore, this section of Farmwald et al discloses that "a request packet and the corresponding bus access are separated by a selected number of bus cycles, allowing the bus to be used in the intervening bus cycles by the same or other masters for additional requests or brief bus accesses."

Sarangdhar et al at column 2, line 63 through column 3, line 17 discloses, among other things, "[a]nother element that may be included is an ownership state indicator that indicates the ownership state of the system bus", "[i]f the ownership state is a first state the symmetric arbitrator of each processor selects the bus owner at least one clock cycle earlier than if the ownership state is a second state", and "[t]he first and second states can be idle and busy states, respectively." The cited section of Sarangdhar et al seems to relate to arbitrating for selection of a bus owner. If the "ownership state indicator" referenced in this section of Sarangdhar et al is in a "first state", the "bus owner" is selected at least one clock cycle earlier than if the ownership state is a second state. The Appellants assert that the reference to the "first state" as "idle" and the "second state" as "busy" relates to column 9, lines 19-22 of Sarangdhar et al which discloses "a symmetric ownership state bit that describes whether the bus ownership is being retained by the current symmetric owner ("busy" state) or is in a state where no symmetric agent currently owns the bus ("idle" state)."

The "request packet " and the corresponding text in Farmwald et al referenced by the Examiner does not disclose scheduling a transaction including usage of a bus by setting a first plurality of bits to a level, with each of the first plurality of bits set to the level indicating the usage of the bus during a corresponding one of a first plurality of clock cycles to occur. Rather, as indicated in the sections of Farmwald et al cited above the "request packet" is used by each slave on the bus must to determine if that slave needs to respond to the packet and if so respond by returning one or more bytes of data or by storing information made available from the bus. Furthermore, the "bus-busy" data structure and associated text disclosed in Farmwald et al at column 12, line 56 through column 13, line 3 does not disclose scheduling a transaction including usage of a bus by setting a first plurality of bits to a level, with each of the first plurality of bits set to the level indicating the usage of the bus during a corresponding one of a first plurality of clock cycles to occur. Rather, this section of Farmwald et al suggests, in generalized, relatively non-specific terms, that each master could keep track of when a bus is and will be busy. Therefore, Farmwald et al does not disclose these limitations of claim 22.

The "ownership state indicator" and corresponding text included in Sarangdhar et al at column 3, lines 11-17 does not disclose a first plurality of bits set to a level, with

each of the first plurality of bits set to the level indicating the usage of the bus during a corresponding one of a first plurality of clock cycles to occur. Rather, the state of the "ownership state indicator" disclosed in Sarangdhar et al determines when the bus owner is selected by the symmetric arbitrator of each processor, not scheduling usage of a bus for a transaction.

Therefore, the rejection of claim 22 under 35 U.S.C. § 103(a) is improper and should be reversed because the prior art references cited in the Examiner's rejection of claim 22 do not teach all the limitations of this claim. Claims 23-26 are dependent upon claim 22 and the rejections of claims 23-26 under 35 U.S.C. § 103(a) based upon Farmwald et al in view of Sarangdhar et al is improper and should be reversed for at least the same reason as discussed for claim 22.

**D. Claim 27 Is Patentable Over Patentable Over Farmwald et al. in View of Sarangdhar et al Because Neither Farmwald et al or Sarangdhar et al Disclose that a first lowest order bit of the first plurality of bits corresponds to a beginning of a first transaction on the bus and a second lowest order bit of the second plurality of bits corresponds to a beginning of a second transaction on the bus.**

Farmwald et al at column 9, lines 21-36 discloses, among other things, a "request packet 22" containing "6 bytes of data—4.5 address bytes and 1.5 control bytes" and discloses that "[s]etting 23 AddrValid=1 in an otherwise unused cycle indicates the start of an request packet (control information)". And, Farmwald et al at column 12, line 56 through column 13, line 3 discloses, among other things, " [a] simple method is for each master to maintain a bus-busy data structure, for example by maintaining two pointers, one to indicate the earliest point in the future when the bus will be busy and the other to indicate the earliest point in the future when the bus will be free, that is, the end of the latest pending data block transfer. Using this information, each master can determine whether and when there is enough time to send a request packet (as described above under Protocol) before the bus becomes busy with another data block transfer and whether the corresponding data block transfer will interfere with pending bus transactions. Thus each master must read every request packet and

update its bus-busy data structure to maintain information about when the bus is and will be free."

Farmwald et al at column 6 line 52 through column 7 line 5 discloses, among other things, initiating "a bus transaction by sending a request packet (a sequence of bytes comprising address and control information) to one or more slave devices on the bus." It additionally discloses that an "address can consist of 16 to 40 or more bits", "each slave on the bus must decode the request packet to see if that slave needs to respond to the packet", and "after a specified access time the slave(s) respond by returning one or more bytes (8 bits) of data or by storing information made available from the bus." Furthermore, this section of Farmwald et al discloses that "a request packet and the corresponding bus access are separated by a selected number of bus cycles, allowing the bus to be used in the intervening bus cycles by the same or other masters for additional requests or brief bus accesses."

Sarangdhar et al at column 2, line 63 through column 3, line 17 discloses, among other things, "[a]nother element that may be included is an ownership state indicator that indicates the ownership state of the system bus", "[i]f the ownership state is a first state the symmetric arbitrator of each processor selects the bus owner at least one clock cycle earlier than if the ownership state is a second state", and "[t]he first and second states can be idle and busy states, respectively." The cited section of Sarangdhar et al seems to relate to arbitrating for selection of a bus owner. If the "ownership state indicator" referenced in this section of Sarangdhar et al is in a "first state", the "bus owner" is selected at least one clock cycle earlier than if the ownership state is a second state. The Appellants assert that the reference to the "first state" as "idle" and the "second state" as "busy" relates to column 9, lines 19-22 of Sarangdhar et al which discloses "a symmetric ownership state bit that describes whether the bus ownership is being retained by the current symmetric owner ("busy" state) or is in a state where no symmetric agent currently owns the bus ("idle" state)."

The "request packet " and the corresponding text in Farmwald et al referenced by the Examiner does not disclose that the request packet includes a first lowest order bit of a first plurality of bits that corresponds to a beginning of a first transaction on the bus. The "request packet " and the corresponding text in Farmwald et al referenced by the

Examiner also does not disclose that the request packet includes a second lowest order bit of the second plurality of bits that corresponds to a beginning of a second transaction on the bus. Rather, as indicated in the sections of Farmwald et al cited above the "request packet" is used by each slave on the bus must to determine if that slave needs to respond to the packet and if so respond by returning one or more bytes of data or by storing information made available from the bus. Furthermore, the "bus-busy" data structure and associated text disclosed in Farmwald et al at column 12, line 56 through column 13, line 3 does not disclose that a first lowest order bit of a first plurality of bits corresponds to a beginning of a first transaction on the bus. Also, the "bus-busy" data structure and associated text disclosed in Farmwald et al at column 12, line 56 through column 13, line 3 does not disclose that a second lowest order bit of the second plurality of bits that corresponds to a beginning of a second transaction on the bus. Rather, this section of Farmwald et al suggests, in generalized, relatively non-specific terms, that each master could keep track of when a bus is and will be busy. Therefore, Farmwald et al does not disclose these limitations of claim 27.

. The "ownership state indicator" and corresponding text included in Sarangdhar et al at column 3, lines 11-17 does not disclose that a first lowest order bit of a first plurality of bits corresponds to a beginning of a first transaction on the bus and does not disclose that a second lowest order bit of the second plurality of bits corresponds to a beginning of a second transaction on the bus. Rather, the state of the "ownership state indicator" disclosed in Sarangdhar et al determines when the bus owner is selected by the symmetric arbitrator of each processor, not when a transaction begins on the bus.

Therefore, the rejection of claim 27 under 35 U.S.C. § 103(a) is improper and should be reversed because the prior art references cited in the Examiner's rejection of claim 27 do not teach all the limitations of this claim.

**E. Claim 28 Is Patentable Over Patentable Over Farmwald et al. in View of Sarangdhar et al Because Neither Farmwald et al or Sarangdhar et al Disclose a first number of the first plurality of bits corresponds to a first length of time of the usage of the bus for a first transaction in terms of clock cycles in the first**

**plurality of clock cycles and a second number of the second plurality of bits corresponds to a second length of time of the usage of the bus for a second transaction in terms of clock cycles in the second plurality of clock cycles.**

Farmwald et al at column 9, lines 21-36 discloses, among other things, a "request packet 22" containing "6 bytes of data—4.5 address bytes and 1.5 control bytes" and discloses that "[s]etting 23 AddrValid=1 in an otherwise unused cycle indicates the start of an request packet (control information)". And, Farmwald et al at column 12, line 56 through column 13, line 3 discloses, among other things, " [a] simple method is for each master to maintain a bus-busy data structure, for example by maintaining two pointers, one to indicate the earliest point in the future when the bus will be busy and the other to indicate the earliest point in the future when the bus will be free, that is, the end of the latest pending data block transfer. Using this information, each master can determine whether and when there is enough time to send a request packet (as described above under Protocol) before the bus becomes busy with another data block transfer and whether the corresponding data block transfer will interfere with pending bus transactions. Thus each master must read every request packet and update its bus-busy data structure to maintain information about when the bus is and will be free."

Farmwald et al at column 6 line 52 through column 7 line 5 discloses, among other things, initiating "a bus transaction by sending a request packet (a sequence of bytes comprising address and control information) to one or more slave devices on the bus." It additionally discloses that an "address can consist of 16 to 40 or more bits", "each slave on the bus must decode the request packet to see if that slave needs to respond to the packet", and "after a specified access time the slave(s) respond by returning one or more bytes (8 bits) of data or by storing information made available from the bus." Furthermore, this section of Farmwald et al discloses that "a request packet and the corresponding bus access are separated by a selected number of bus cycles, allowing the bus to be used in the intervening bus cycles by the same or other masters for additional requests or brief bus accesses."

Sarangdhar et al at column 2, line 63 through column 3, line 17 discloses, among other things, "[a]nother element that may be included is an ownership state indicator

that indicates the ownership state of the system bus", "[i]f the ownership state is a first state the symmetric arbitrator of each processor selects the bus owner at least one clock cycle earlier than if the ownership state is a second state", and "[t]he first and second states can be idle and busy states, respectively." The cited section of Sarangdhar et al seems to relate to arbitrating for selection of a bus owner. If the "ownership state indicator" referenced in this section of Sarangdhar et al is in a "first state", the "bus owner" is selected at least one clock cycle earlier than if the ownership state is a second state. The Appellants assert that the reference to the "first state" as "idle" and the "second state" as "busy" relates to column 9, lines 19-22 of Sarangdhar et al which discloses "a symmetric ownership state bit that describes whether the bus ownership is being retained by the current symmetric owner ("busy" state) or is in a state where no symmetric agent currently owns the bus ("idle" state)."

The "request packet " and the corresponding text in Farmwald et al referenced by the Examiner does not disclose that the request packet includes a first number of the first plurality of bits corresponding to a first length of time of the usage of the bus for a first transaction in terms of clock cycles in the first plurality of clock cycles. The "request packet " and the corresponding text in Farmwald et al referenced by the Examiner also does not disclose that the request packet includes a second number of the second plurality of bits corresponding to a second length of time of the usage of the bus for a second transaction in terms of clock cycles in the second plurality of clock cycles. Rather, as indicated in the sections of Farmwald et al cited above the "request packet" is used by each slave on the bus must to determine if that slave needs to respond to the packet and if so respond by returning one or more bytes of data or by storing information made available from the bus.

Furthermore, the "bus-busy" data structure and associated text disclosed in Farmwald et al at column 12, line 56 through column 13, line 3 does not disclose that a first number of the first plurality of bits corresponds to a first length of time of the usage of the bus for a first transaction in terms of clock cycles in the first plurality of clock cycles. Also, the "bus-busy" data structure and associated text disclosed in Farmwald et al at column 12, line 56 through column 13, line 3 does not disclose that a second number of the second plurality of bits corresponds to a second length of time of the

usage of the bus for a second transaction in terms of clock cycles in the second plurality of clock cycles. Rather, this section of Farmwald et al suggests, in generalized, relatively non-specific terms, that each master could keep track of when a bus is and will be busy. Therefore, Farmwald et al does not disclose these limitations of claim 28.

The "ownership state indicator" and corresponding text included in Sarangdhar et al at column 3, lines 11-17 does not disclose that a first number of the first plurality of bits corresponds to a first length of time of the usage of the bus for a first transaction in terms of clock cycles in the first plurality of clock cycles and does not disclose that a second number of the second plurality of bits corresponding to a second length of time of the usage of the bus for a second transaction in terms of clock cycles in the second plurality of clock cycles. Rather, the state of the "ownership state indicator" disclosed in Sarangdhar et al determines when the bus owner is selected by the symmetric arbitrator of each processor, not a length of time of usage of the bus for a transaction in terms of clock cycles.

Therefore, the rejection of claim 28 under 35 U.S.C. § 103(a) is improper and should be reversed because the prior art references cited in the Examiner's rejection of claim 28 do not teach all the limitations of this claim.

**F. Claim 32 Is Patentable Over Patentable Over Farmwald et al. in View of Sarangdhar et al Because Neither Farmwald et al or Sarangdhar et al Disclose a means for determining a value including a plurality of bits, with those of the plurality of bits at a first level indicating usage of a bus during a first set of corresponding clock cycles and with those of the plurality of bits at a second level indicating no usage of the bus during a second set of corresponding clock cycles.**

Farmwald et al at column 9, lines 21-36 discloses, among other things, a "request packet 22" containing "6 bytes of data—4.5 address bytes and 1.5 control bytes" and discloses that "[s]etting 23 AddrValid=1 in an otherwise unused cycle indicates the start of an request packet (control information)". And, Farmwald et al at column 12, line 56 through column 13, line 3 discloses, among other things, " [a] simple method is for each master to maintain a bus-busy data structure, for example by

maintaining two pointers, one to indicate the earliest point in the future when the bus will be busy and the other to indicate the earliest point in the future when the bus will be free, that is, the end of the latest pending data block transfer. Using this information, each master can determine whether and when there is enough time to send a request packet (as described above under Protocol) before the bus becomes busy with another data block transfer and whether the corresponding data block transfer will interfere with pending bus transactions. Thus each master must read every request packet and update its bus-busy data structure to maintain information about when the bus is and will be free."

Farmwald et al at column 6 line 52 through column 7 line 5 discloses, among other things, initiating "a bus transaction by sending a request packet (a sequence of bytes comprising address and control information) to one or more slave devices on the bus." It additionally discloses that an "address can consist of 16 to 40 or more bits", "each slave on the bus must decode the request packet to see if that slave needs to respond to the packet", and "after a specified access time the slave(s) respond by returning one or more bytes (8 bits) of data or by storing information made available from the bus." Furthermore, this section of Farmwald et al discloses that "a request packet and the corresponding bus access are separated by a selected number of bus cycles, allowing the bus to be used in the intervening bus cycles by the same or other masters for additional requests or brief bus accesses."

Sarangdhar et al at column 2, line 63 through column 3, line 17 discloses, among other things, "[a]nother element that may be included is an ownership state indicator that indicates the ownership state of the system bus", "[i]f the ownership state is a first state the symmetric arbitrator of each processor selects the bus owner at least one clock cycle earlier than if the ownership state is a second state", and "[t]he first and second states can be idle and busy states, respectively." The cited section of Sarangdhar et al seems to relate to arbitrating for selection of a bus owner. If the "ownership state indicator" referenced in this section of Sarangdhar et al is in a "first state", the "bus owner" is selected at least one clock cycle earlier than if the ownership state is a second state. The Appellants assert that the reference to the "first state" as "idle" and the "second state" as "busy" relates to column 9, lines 19-22 of Sarangdhar et

al which discloses "a symmetric ownership state bit that describes whether the bus ownership is being retained by the current symmetric owner ("busy" state) or is in a state where no symmetric agent currently owns the bus ("idle" state)."

The Appellants assert that in the sections of Farmwald et al cited above, there is no disclosure of the functions recited for the "means for determining a value" element and no structure disclosed in the sections of Farmwald et al cited above that perform these functions. The disclosure associated with the "request packet 22" in the above cited sections of Farmwald et al does not disclose the function of determining a value including a plurality of bits, with those of the plurality of bits at a first level indicating usage of a bus during a first set of corresponding clock cycles and with those of the plurality of bits at a second level indicating no usage of the bus during a second set of corresponding clock cycles. The bits associated with the "request packet 22" comprise address and control information to instruct a slave on a bus to carry out a requested bus transaction at the requested time. The bits associated with the "request packet 22" at a first level do not indicate usage of the bus during clock cycles corresponding to those of the bits at the first level and the bits associated with the "request packet 22" at a second level do not indicate no usage of the bus during clock cycles corresponding to those of the bits at the second level. Furthermore, the disclosure associated with the "request packet 22" in the above cited sections of Farmwald et al does not disclose structure to perform this function of claim 32 recited above in this paragraph. Rather, as indicated in the sections of Farmwald et al cited above the "request packet" is used by each slave on the bus must to determine if that slave needs to respond to the packet and if so respond by returning one or more bytes of data or by storing information made available from the bus.

Furthermore, the "bus-busy" data structure and associated text disclosed in Farmwald et al at column 12, line 56 through column 13, line 3 does not disclose a means for determining a value including a plurality of bits, with those of the plurality of bits at a first level indicating usage of a bus during a first set of corresponding clock cycles and with those of the plurality of bits at a second level indicating no usage of the bus during a second set of corresponding clock cycles. Rather, this section of Farmwald et al suggests, in generalized, relatively non-specific terms, that each master could keep

track of when a bus is and will be busy. Therefore, Farmwald et al does not disclose these limitations of claim 32.

The "ownership state indicator" and corresponding text included in Sarangdhar et al at column 3, lines 11-17 does not disclose that the processor determines an "ownership state indicator" including a plurality of bits, with those of the plurality of bits in the "ownership state indicator" at a first level indicating usage of a bus during a first set of corresponding clock cycles and with those of the plurality of bits at a second level indicating no usage of the bus during a second set of corresponding clock cycles. Rather, the state of the "ownership state indicator" disclosed in Sarangdhar et al determines when the bus owner is selected by the symmetric arbitrator of each processor, not structure for determining bits indicating usage of a bus during corresponding clock cycles.

Therefore, the rejection of claim 32 under 35 U.S.C. § 103(a) is improper and should be reversed because the prior art references cited in the Examiner's rejection of claim 32 do not teach all the limitations of this claim.

**G. Claim 34 Is Patentable Over Patentable Over Farmwald et al. in View of Sarangdhar et al Because Neither Farmwald et al or Sarangdhar et al Disclose the means for determining a value including a configuration to change the plurality of bits in the storage device according to occurrence of ones of the first set of corresponding clock cycles and ones of the second set of corresponding cycles.**

Farmwald et al at column 9, lines 21-36 discloses, among other things, a "request packet 22" containing "6 bytes of data—4.5 address bytes and 1.5 control bytes" and discloses that "[s]etting 23 AddrValid=1 in an otherwise unused cycle indicates the start of an request packet (control information)". And, Farmwald et al at column 12, line 56 through column 13, line 3 discloses, among other things, " [a] simple method is for each master to maintain a bus-busy data structure, for example by maintaining two pointers, one to indicate the earliest point in the future when the bus will be busy and the other to indicate the earliest point in the future when the bus will be

free, that is, the end of the latest pending data block transfer. Using this information, each master can determine whether and when there is enough time to send a request packet (as described above under Protocol) before the bus becomes busy with another data block transfer and whether the corresponding data block transfer will interfere with pending bus transactions. Thus each master must read every request packet and update its bus-busy data structure to maintain information about when the bus is and will be free."

Farmwald et al at column 6 line 52 through column 7 line 5 discloses, among other things, initiating "a bus transaction by sending a request packet (a sequence of bytes comprising address and control information) to one or more slave devices on the bus." It additionally discloses that an "address can consist of 16 to 40 or more bits", "each slave on the bus must decode the request packet to see if that slave needs to respond to the packet", and "after a specified access time the slave(s) respond by returning one or more bytes (8 bits) of data or by storing information made available from the bus." Furthermore, this section of Farmwald et al discloses that "a request packet and the corresponding bus access are separated by a selected number of bus cycles, allowing the bus to be used in the intervening bus cycles by the same or other masters for additional requests or brief bus accesses."

Sarangdhar et al at column 2, line 63 through column 3, line 17 discloses, among other things, "[a]nother element that may be included is an ownership state indicator that indicates the ownership state of the system bus", "[i]f the ownership state is a first state the symmetric arbitrator of each processor selects the bus owner at least one clock cycle earlier than if the ownership state is a second state", and "[t]he first and second states can be idle and busy states, respectively." The cited section of Sarangdhar et al seems to relate to arbitrating for selection of a bus owner. If the "ownership state indicator" referenced in this section of Sarangdhar et al is in a "first state", the "bus owner" is selected at least one clock cycle earlier than if the ownership state is a second state. The Appellants assert that the reference to the "first state" as "idle" and the "second state" as "busy" relates to column 9, lines 19-22 of Sarangdhar et al which discloses "a symmetric ownership state bit that describes whether the bus

ownership is being retained by the current symmetric owner ("busy" state) or is in a state where no symmetric agent currently owns the bus ("idle" state)."

The Appellants assert that in the sections of Farmwald et al cited above, there is no disclosure that the "request packet 22" or its associated structure disclosed in the cited sections of Farmwald et al includes a configuration to change the plurality of bits in a storage device according to occurrence of ones of a first set of corresponding clock cycles and ones of a second set of corresponding cycles. The bits associated with the "request packet 22" comprise address and control information to instruct a slave on a bus to carry out a requested bus transaction at the requested time. The master device, as disclosed in the cited sections of Farmwald et al, that initiates a bus transaction by sending a request packet does not perform the function of changing bits of the "request packet 22" according to occurrence of clock cycles corresponding to the bits of the "request packet 22". Furthermore, the disclosure associated with the "request packet 22" in the above cited sections of Farmwald et al does not disclose structure to perform this function of claim 34 recited above in this paragraph. Rather, as indicated in the sections of Farmwald et al cited above, a particular "request packet", once sent for a bus transaction by the master device, does not appear to be changed by the master device.

Furthermore, the "bus-busy" data structure and associated text disclosed in Farmwald et al at column 12, line 56 through column 13, line 3 does not disclose changing bits of the "bus-busy" data structure according to occurrence of clock cycles corresponding to the bits of the "bus-busy" data structure. Rather, this section of Farmwald et al suggests, in generalized, relatively non-specific terms, that each master could keep track of when a bus is and will be busy. Therefore, Farmwald et al does not disclose these limitations of claim 34.

The "ownership state indicator" and corresponding text included in Sarangdhar et al at column 3, lines 11-17 does not disclose changing the "ownership state indicator" according to occurrence of ones of the first set of corresponding clock cycles and ones of the second set of corresponding cycles. Rather, the state of the "ownership state indicator" disclosed in Sarangdhar et al determines when the bus owner is selected by

the symmetric arbitrator of each processor, not structure for determining bits indicating usage of a bus during corresponding clock cycles.

Therefore, the rejection of claim 34 under 35 U.S.C. § 103(a) is improper and should be reversed because the prior art references cited in the Examiner's rejection of claim 34 do not teach all the limitations of this claim.

## Conclusion

In view of the foregoing, the Appellants submit that Claims 2-6 and 11 are not properly rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,032,214 issued to Farmwald et al and are therefore patentable. Claims 7-9, 12 and 22-34 are not properly rejected under 35 U.S.C. § 103(a) over Farmwald et al in view of U.S. Patent No. 5,581,782 issued to Saranghdhar et al and are therefore patentable. Accordingly, Appellant respectfully requests that the Board reverse all claim rejections and indicate that a Notice of Allowance respecting all pending claims should be issued.

**Summary**

For the foregoing reasons, it is submitted that the Examiner's rejections are erroneous, and reversal of the implied rejections is respectfully requested.

Dated this 8 day of August, 2005.

Respectfully submitted,

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## APPENDIX - THE CLAIMS ON APPEAL

2.(previously presented) A method for performing a transaction on a bus, comprising:

receiving a signal requesting the transaction;

generating a first value using the signal;

storing the first value in a storage device, with the first value including a plurality of bits and with those of the plurality of bits in a first state corresponding to clock cycles during which the usage of the bus occurs for the transaction; and

executing the transaction according to the first value.

3.(original) The method as recited in claim 2, wherein:

each of the storage elements stores one of the plurality of bits.

4.(original) The method as recited in claim 3, wherein:

receiving the signal includes receiving a second value indicating a number of the clock cycles during which the usage of the bus occurs for the transaction;

generating the first value includes generating the plurality of bits using the second value with positions within the first value of those of the plurality of bits in the first state indicating the clock cycles during which the usage of the bus occurs for the transaction; and

each of the positions within the first value corresponds to one of the storage elements.

5.(original) The method as recited in claim 4, further comprising:

changing the first value in the storage device after storing the first value and after an occurrence of at least one of the clock cycles by shifting ones of the plurality of bits between the storage elements.

6.(original) The method as recited in claim 5, wherein:

executing the transaction includes monitoring a first one of the positions to determine a beginning of the transaction.

7.(original) The method as recited in claim 6, wherein:

those of the plurality of bits in a second state indicate the clock cycles during which the bus exists in an idle condition; and

generating the first value includes generating the plurality of bits in the second state so that the bus exists in the idle condition for at least one of the clock cycles between the usage of the bus for the transaction and the usage of the bus for a previous transaction.

8.(original) The method as recited in claim 7, wherein:

the bus includes a data bus;

the transaction includes an access to a memory device including a control phase and a data phase;

executing the transaction includes beginning the control phase when the first one of the positions enters the second state; and

executing the transaction includes beginning the data phase when a second one of the positions enters the first state.

9.(original) The method as recited in claim 7, wherein:

the bus includes an address bus;

the transaction includes an access to a memory device including a control phase;

executing the transaction includes beginning the control phase when the

the first one of the positions enters the first state.

11.(previously presented) A system, comprising:

a bus;

a processor configured to receive first data from the bus;

a first memory device configured to send the first data to the bus;

a memory controller coupled to the processor and the memory device and configured to control transfer of the first data over the bus; and

a bus management device arranged to receive a first value from the memory controller indicating a number of clock cycles with the first data on the bus and including a storage device to store a second value including a first plurality of bits, with positions within the second value of those of the first plurality of bits in a first state corresponding to clock cycles during which the first data exists on the bus .

12.(original) The system as recited in claim 11, wherein:

those of the first plurality of bits in a second state indicate the clock cycles during which the bus exists in an idle condition; and

the bus management device includes a configuration to detect a change in one of the positions within the second value from the first state to the second state and to signal the memory controller to begin a first access to the first memory device a first time period before the clock cycles corresponding to those of the first plurality of bits in the first state begin.

22.(previously presented) A method, comprising:

scheduling a first transaction including usage of a bus by setting a first plurality of bits to a level, with each of the first plurality of bits set to the level indicating the usage of the bus during a corresponding one of a first plurality clock cycles to occur; and

scheduling a second transaction including usage of the bus by setting a second plurality of bits to the level, with each of the second plurality of bits set to the level indicating the usage of the bus during a corresponding one of a second plurality of clock cycles to occur after the first plurality of clock cycles.

23.(previously presented) The method as recited in claim 22, wherein:

the second plurality of clock cycles occurs at least one clock cycle after the first plurality of clock cycles.

24.(previously presented) The method as recited in claim 22, further comprising:

storing the first plurality of bits in a storage device; and

storing the second plurality of bits in the storage device.

25.(previously presented) The method as recited in claim 24, wherein:

the storage device includes a plurality of storage elements, with the storing the first plurality of bits and the storing the second plurality of bits including storing ones of the first plurality of bits and ones of the second plurality of bits in individual of the plurality of storage elements.

26.(previously presented) The method as recited in claim 25, further comprising:

with the storage device including a shift register, shifting the first plurality of bits and the second plurality of bits in the shift register corresponding to the occurrence of one of a clock cycle in the first plurality of clock cycles.

27.(previously presented) The method as recited in claim 26, wherein:

a first lowest order bit of the first plurality of bits corresponds to a beginning of a first transaction on the bus; and

a second lowest order bit of the second plurality of bits corresponds to a beginning of a second transaction on the bus.

28.(previously presented) The method as recited in claim 22, wherein:

a first number of the first plurality of bits corresponds to a first length of time of the usage of the bus for a first transaction in terms of clock cycles in the first plurality of clock cycles; and

a second number of the second plurality of bits corresponds to a second length of time of the usage of the bus for a second transaction in terms of clock cycles in the second plurality of clock cycles.

29.(previously presented) The method as recited in claim 22, wherein:

the first transaction includes accessing a first memory device;

the second transaction includes accessing a second memory device;

the first plurality of clock cycles includes a first number of the clock cycles corresponding to the first memory device having a first access time; and

the second plurality of clock cycles includes a second number of the clock cycles corresponding to the second memory device having a second access time.

30.(previously presented) The method as recited in claim 29, wherein:

scheduling the first transaction includes determining the first access time; and

scheduling the second transaction includes determining the second access time.

31. (previously presented) The method as recited in claim 22, wherein:

the bus includes a data bus;

the first transaction includes accessing a first memory device; and

the second transaction includes accessing a second memory device with application of address information to an address bus occurring during the usage of the data bus during the first transaction.

32.(previously presented) An apparatus, comprising:

means for determining a value including a plurality of bits, with those of the plurality of bits at a first level indicating usage of a bus during a first set of corresponding clock cycles and with those of the plurality of bits at a second level indicating no usage of the bus during a second set of corresponding clock cycles; and

a storage device to store the plurality of bits.

33.(previously presented) The apparatus as recited in claim 32, wherein:

the usage of the bus during the first set of the corresponding clock cycles corresponds to accessing a memory device; and

the means for determining a value includes a configuration to determine a number of clock cycles included in the first set for accessing the memory device.

34.(previously presented) The apparatus as recited in claim 32, wherein:

the means for determining a value includes a configuration to change the plurality of bits in the storage device according to occurrence of ones of the first set of corresponding clock cycles and ones of the second set of corresponding cycles.